Fig. 1

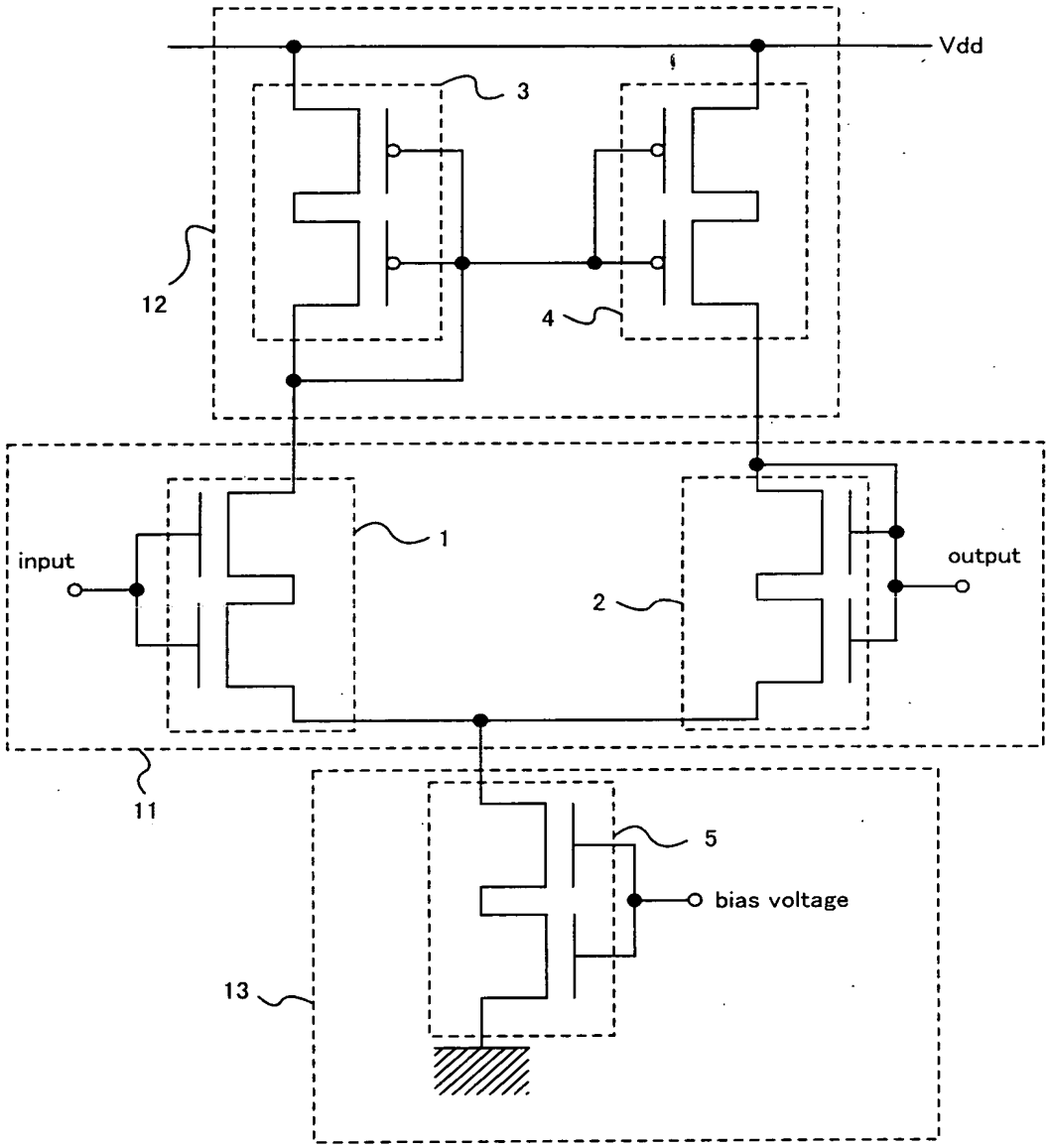


Fig. 2

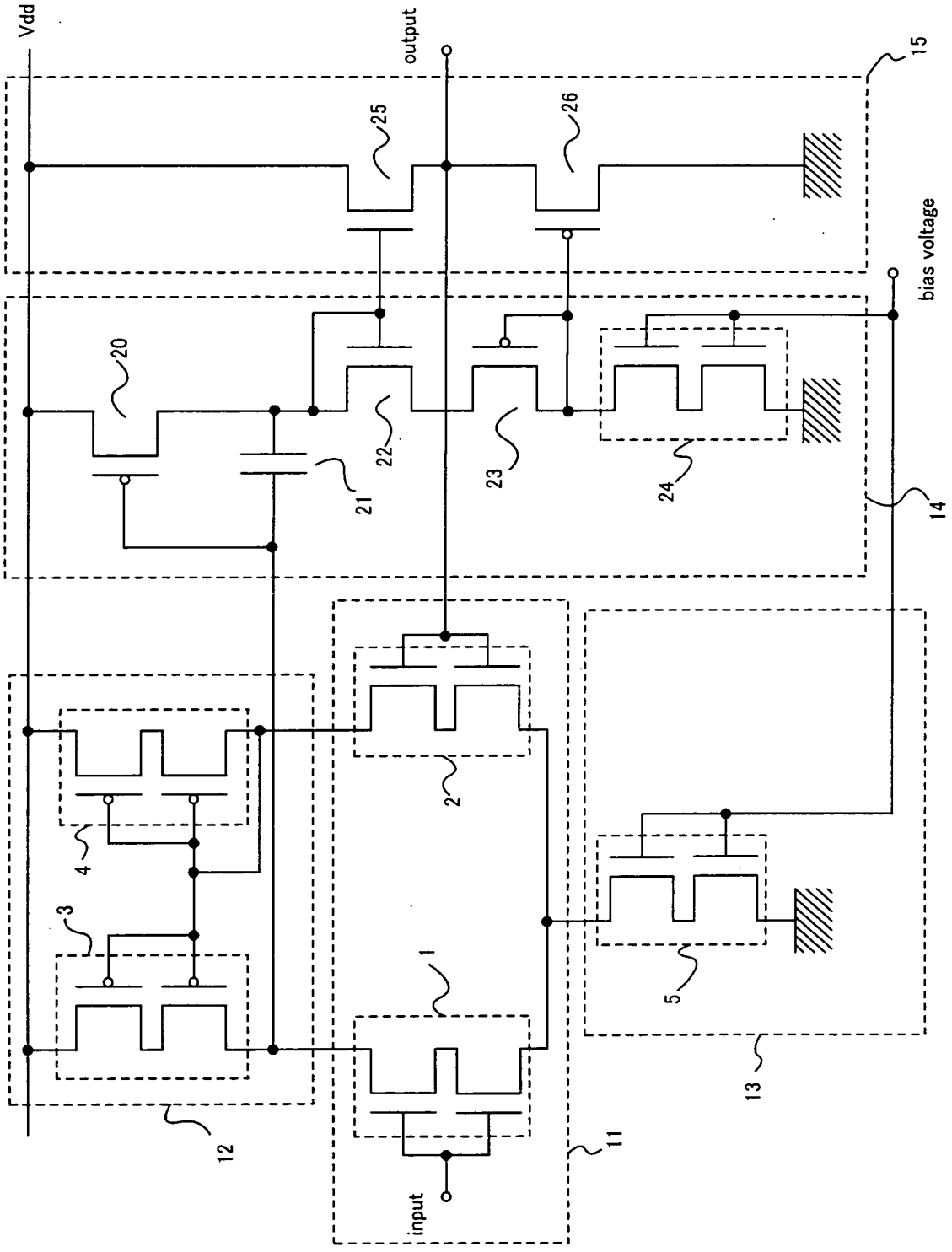

Vdd
output
bias voltage
input
1
2
3
4
5
11
12
13
14
15
20
21
22
23
24
25
26

Fig. 3

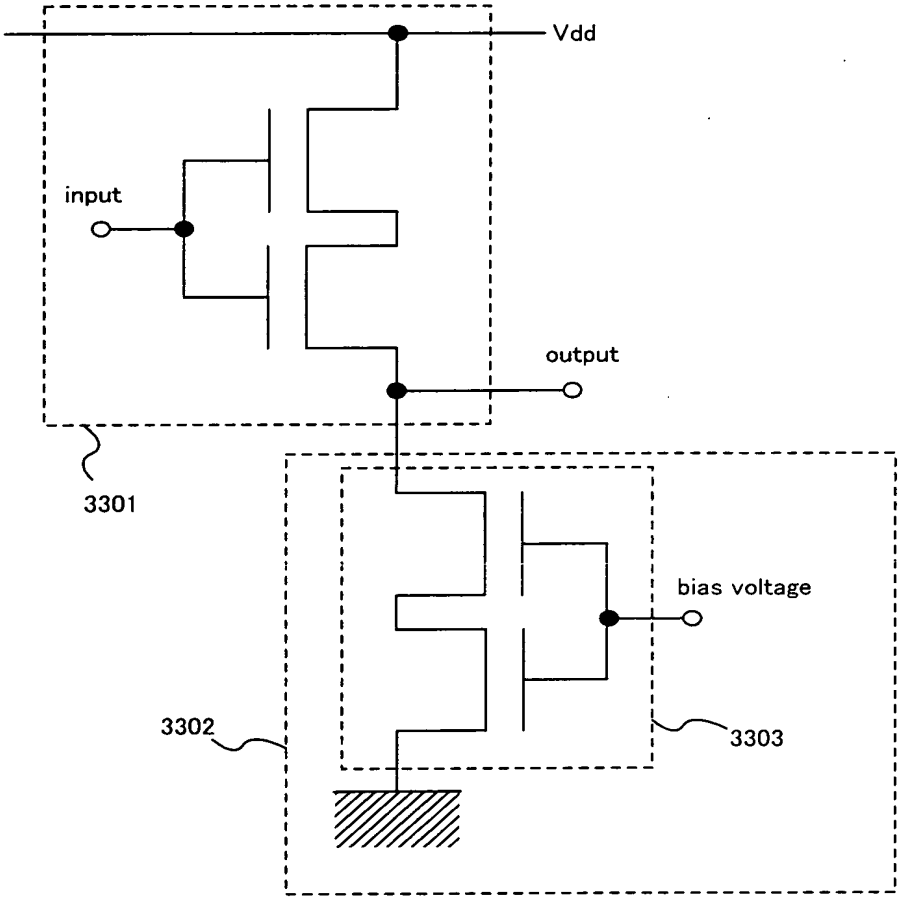
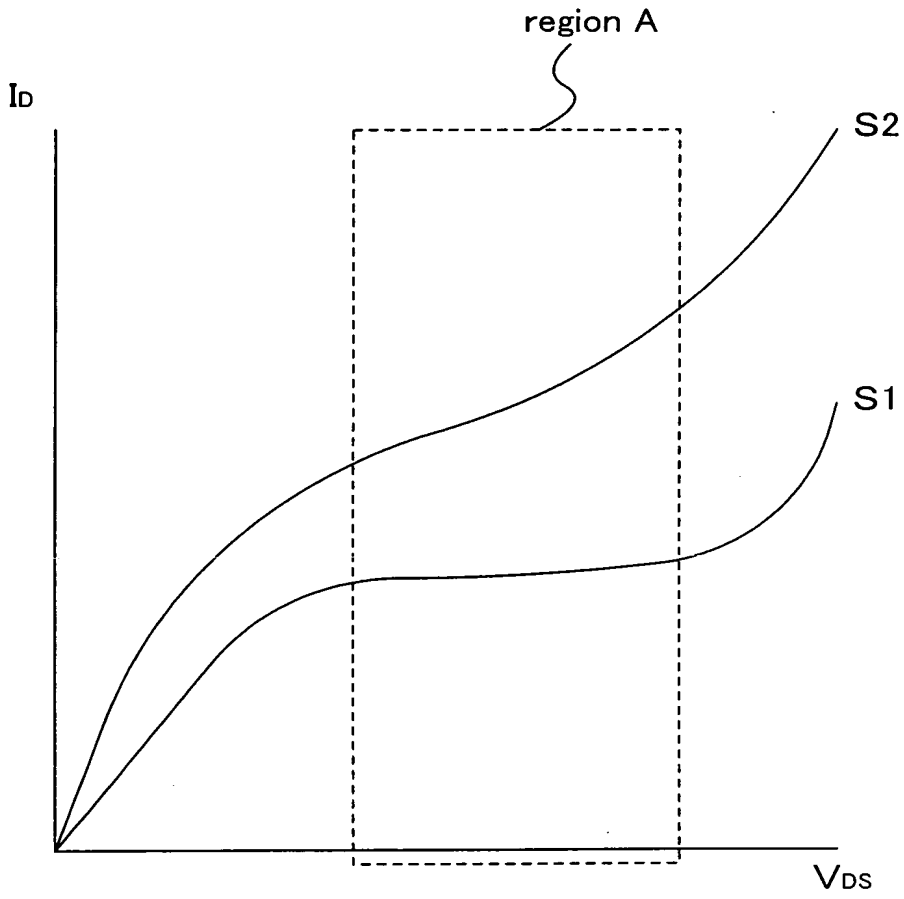


Fig. 4



Prior

Fig. 5

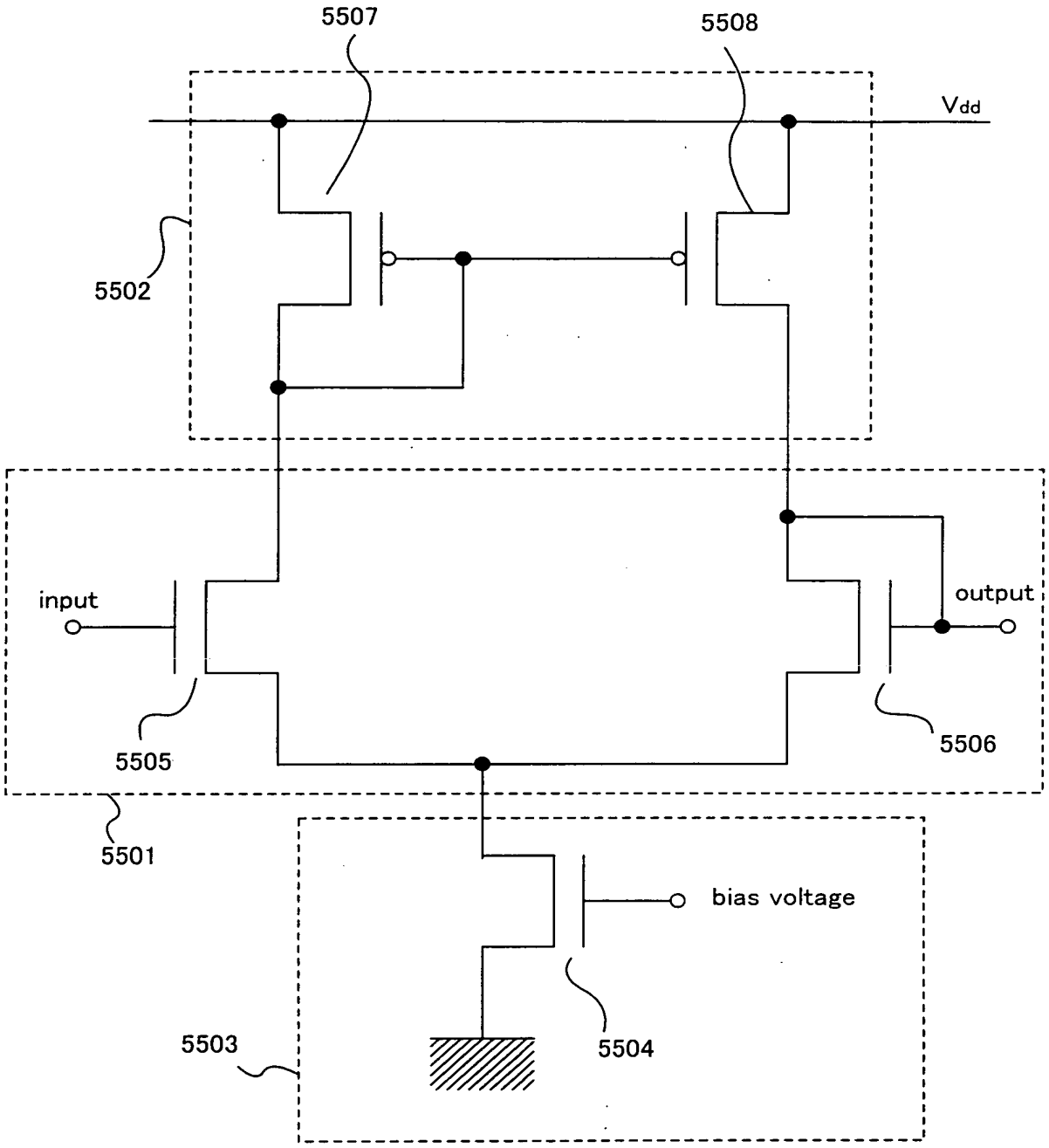

5507
5508
Vdd
5502
input
output
5505
5506
5501
bias voltage
5503
5504

Fig. 6 Prior

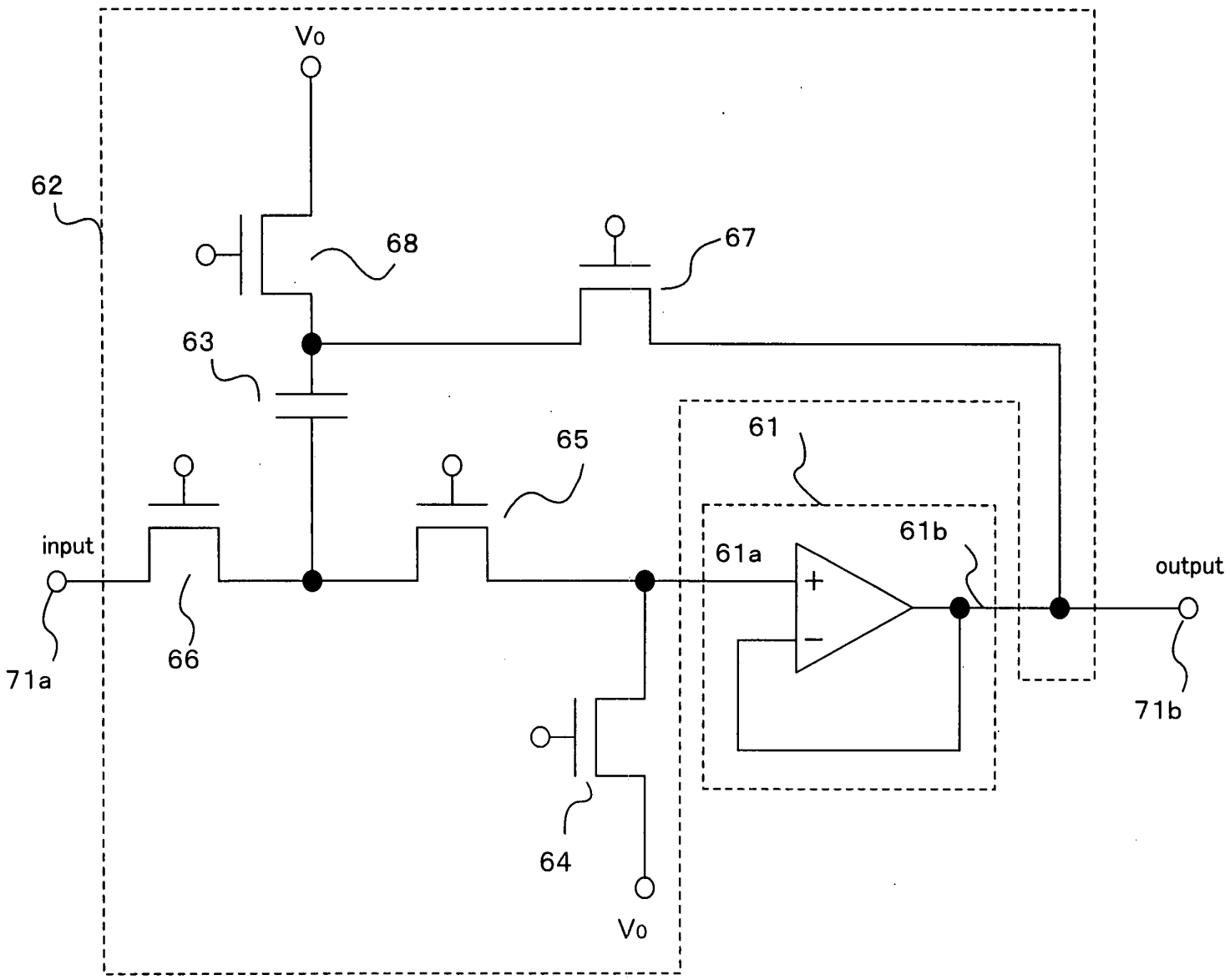


Fig. 7

Prior

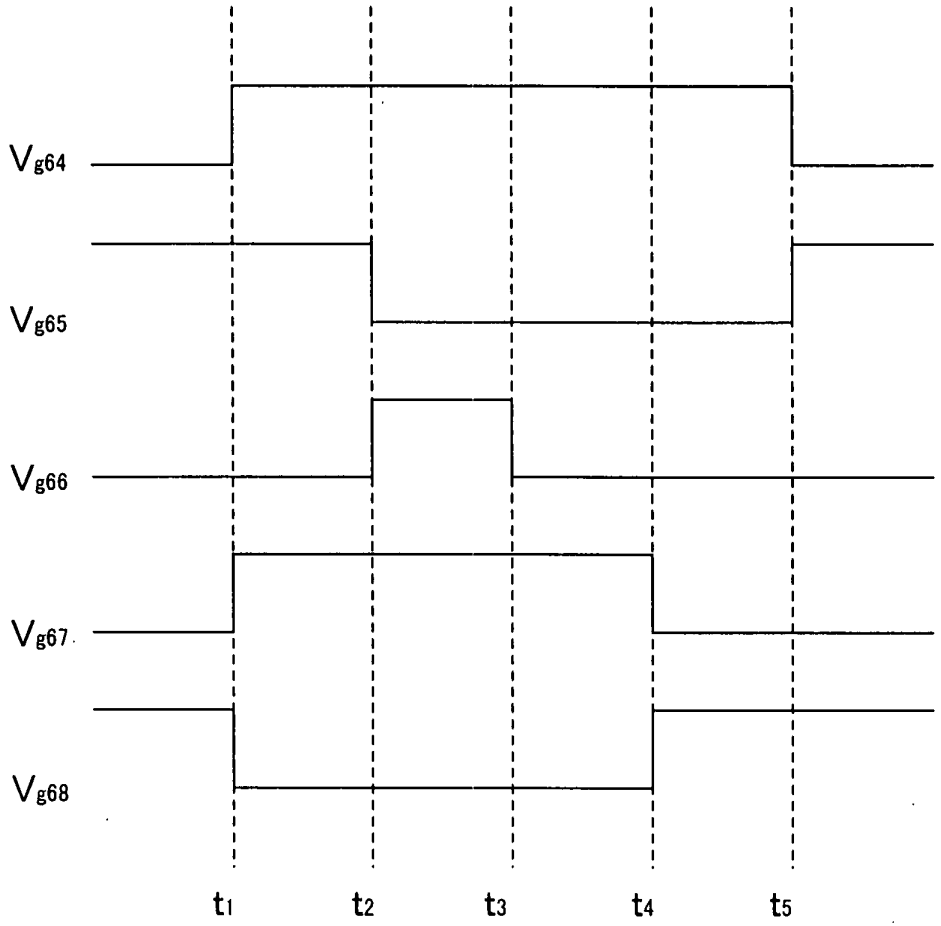


Fig. 8

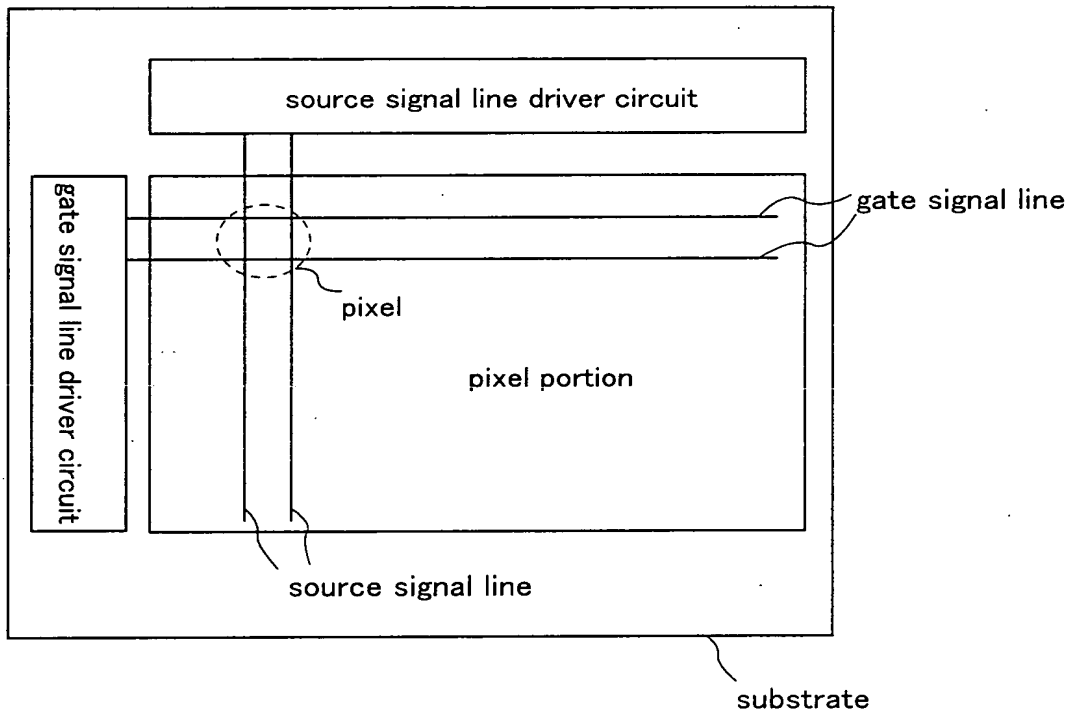

source signal line driver circuit
gate signal line driver circuit
gate signal line
pixel
pixel portion
source signal line
substrate

Fig. 9

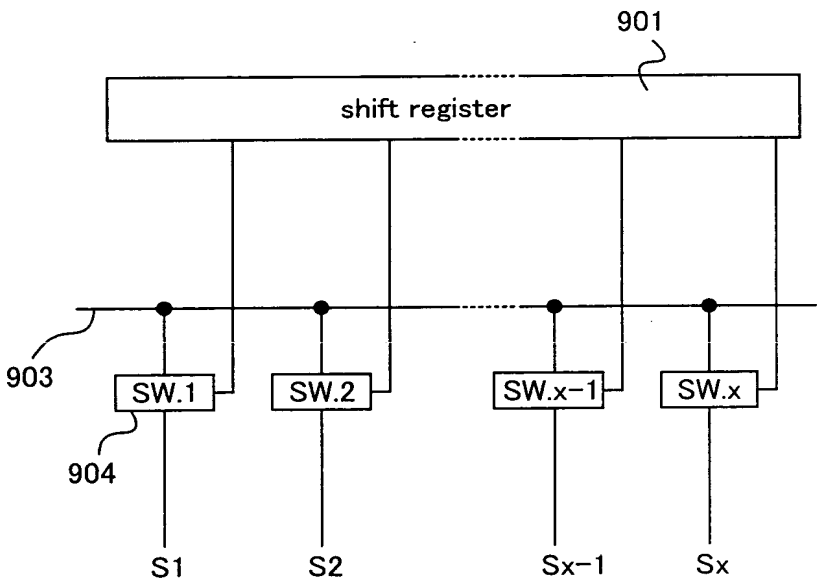


Fig. 10

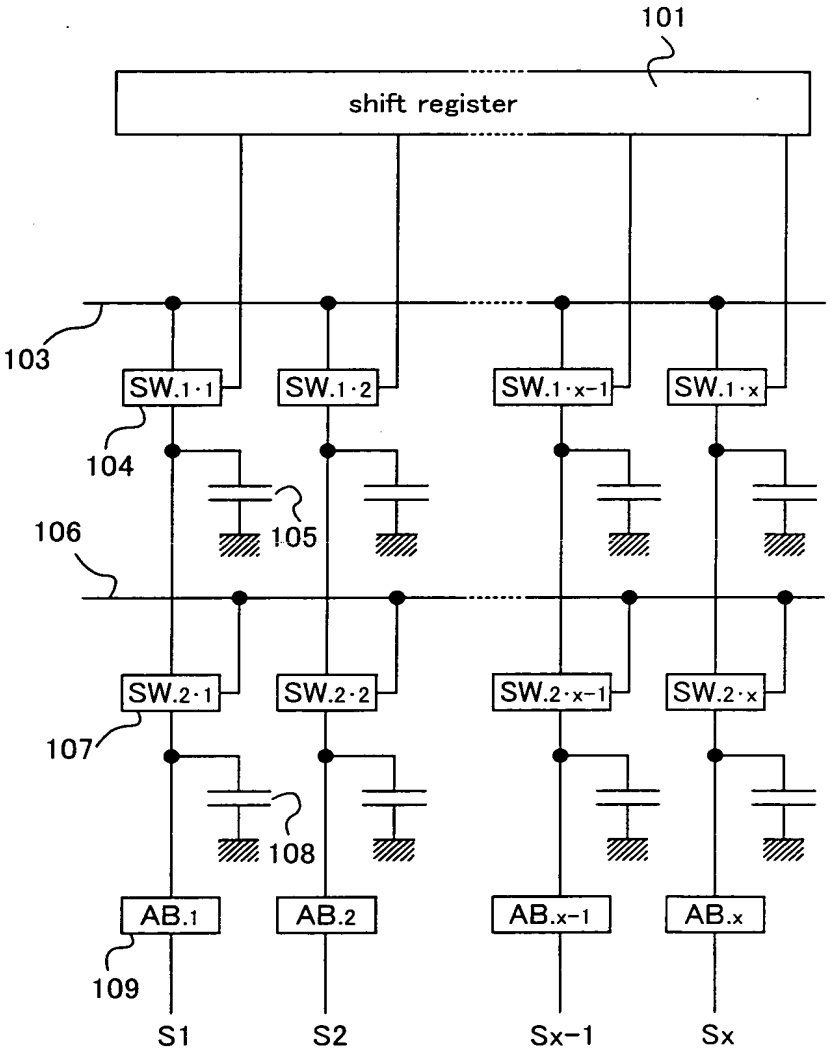

101
shift register
103
SW.1·1
SW.1·2
SW.1·x-1
SW.1·x
104
105
106
SW.2·1
SW.2·2
SW.2·x-1
SW.2·x
107
108
AB.1
AB.2
AB.x-1
AB.x
109
S1
S2
Sx-1
Sx

Fig. 11A

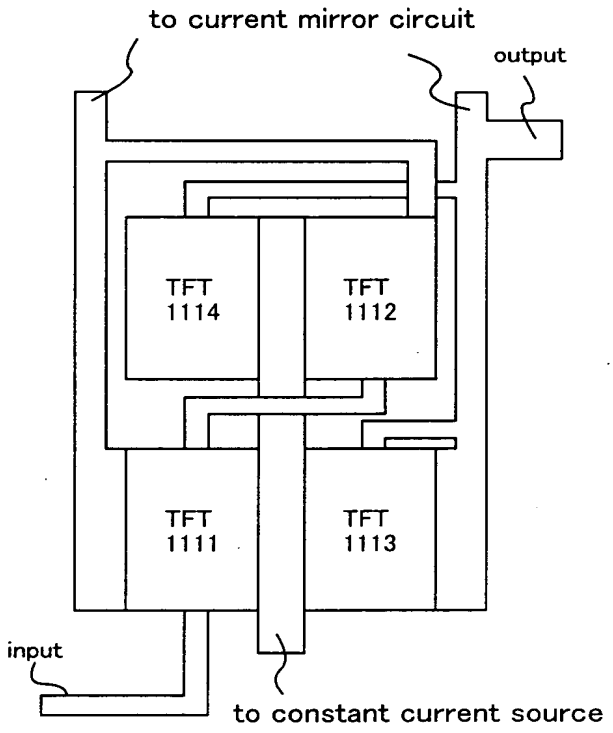


Fig. 11B

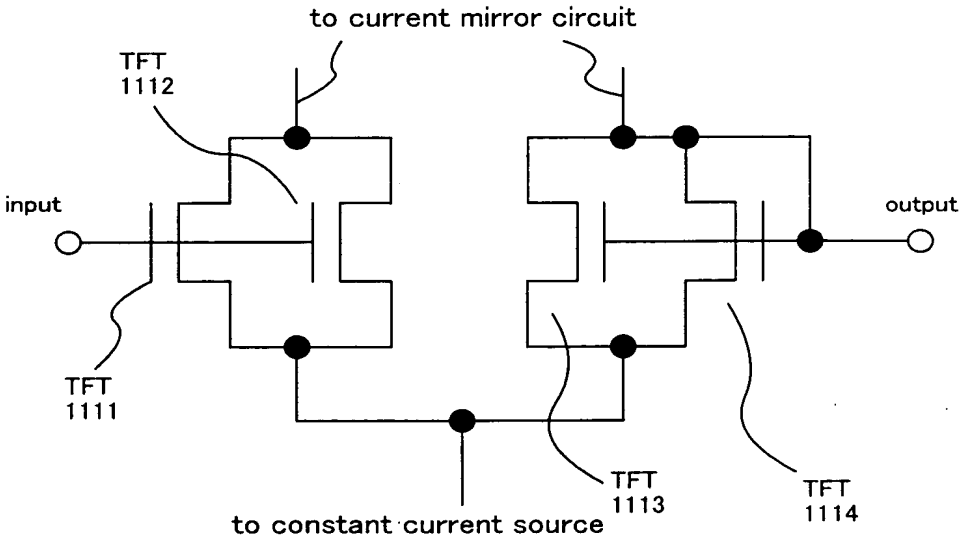


Fig. 12

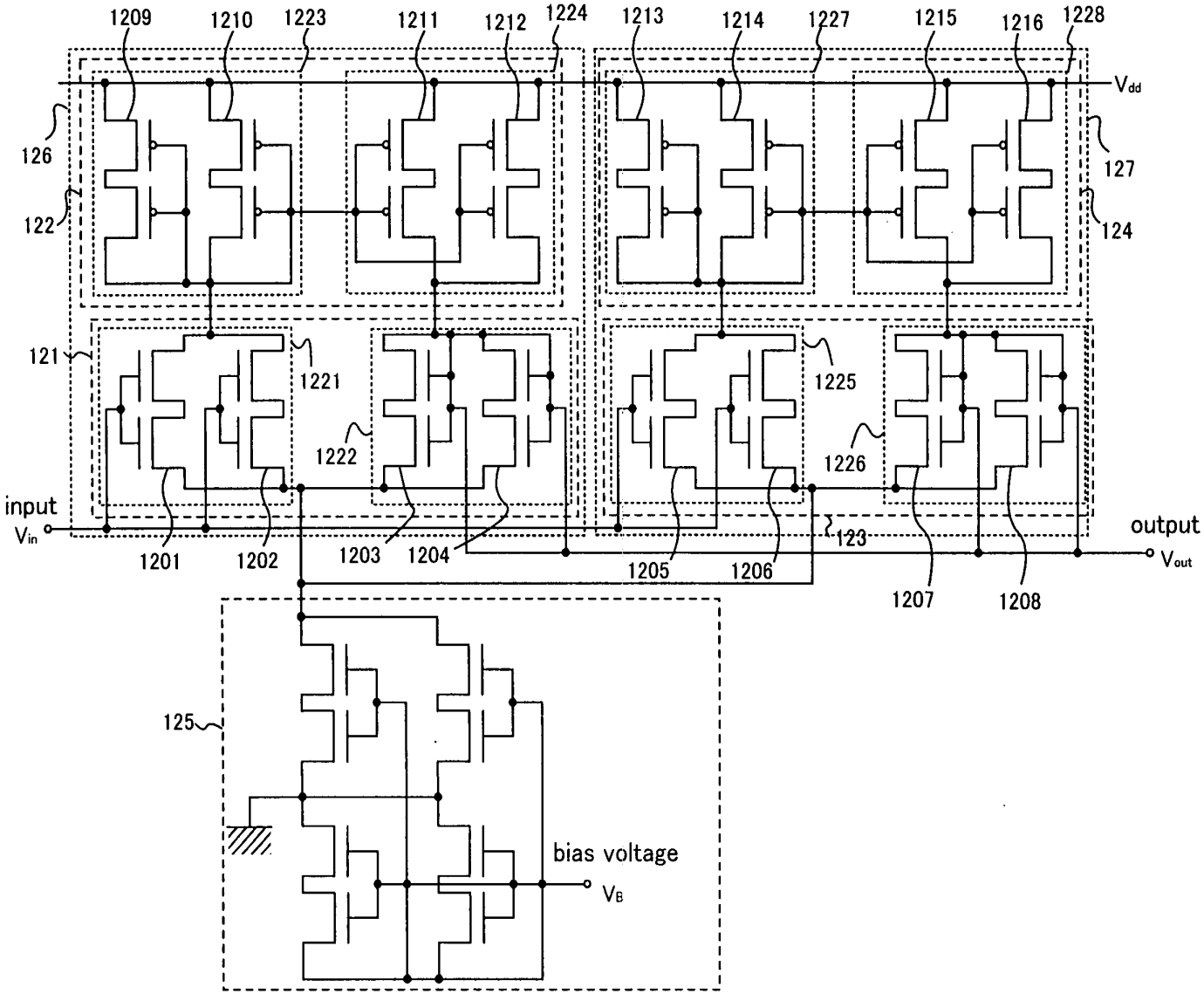

1209
1210
1223
1211
1212
1224
1213
1214
1227
1215
1216
1228
Vdd
126
127
122
124
121
1221
1225
1222
1226
input
Vin
output
Vout
123
1201
1202
1203
1204
1205
1206
1207
1208
125
bias voltage
VB

Fig. 13

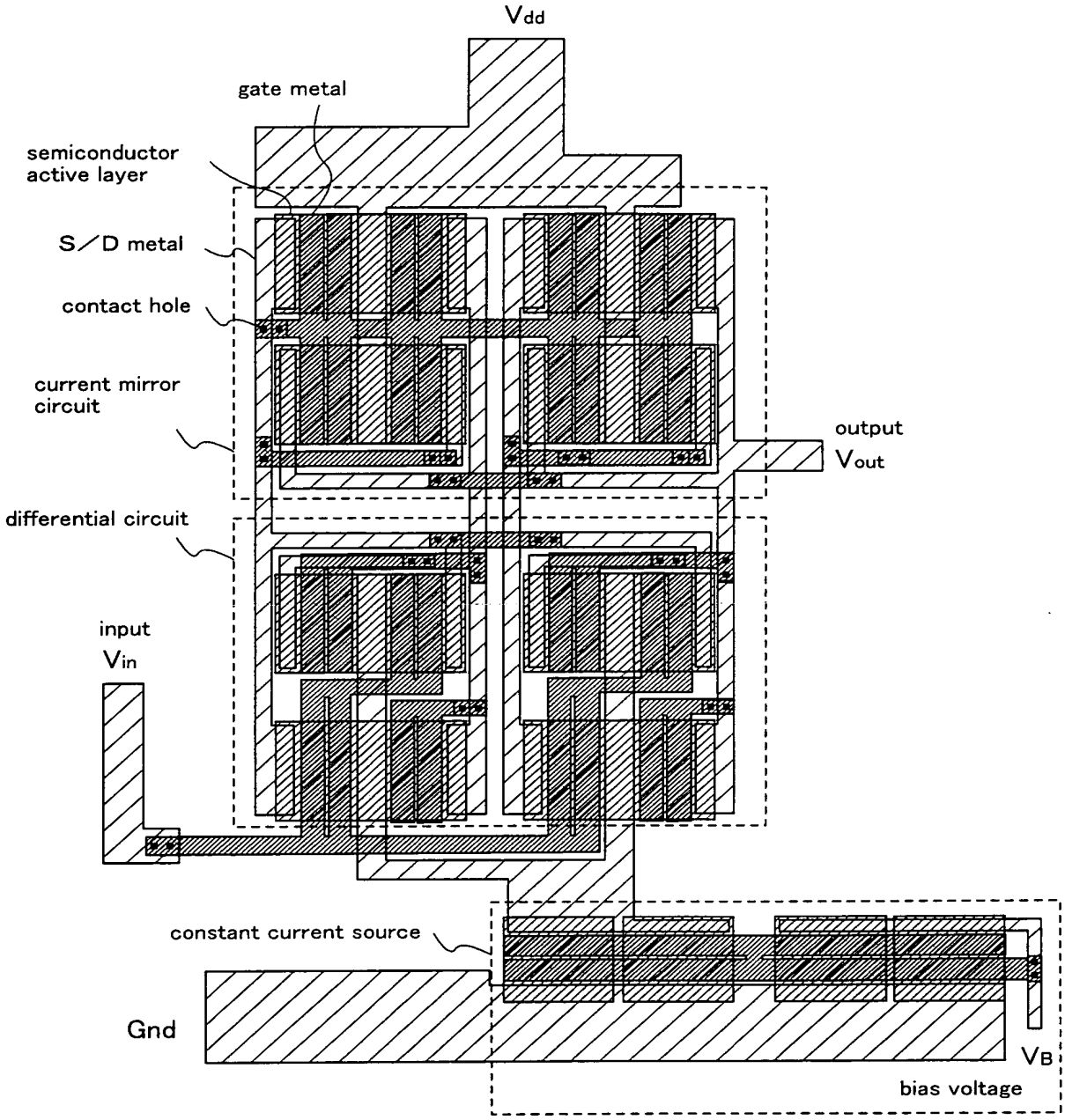

Vdd
gate metal
semiconductor
active layer
S／D metal
contact hole
current mirror
circuit
output
Vout
differential circuit
input
Vin
constant current source
Gnd
VB
bias voltage

Fig. 14

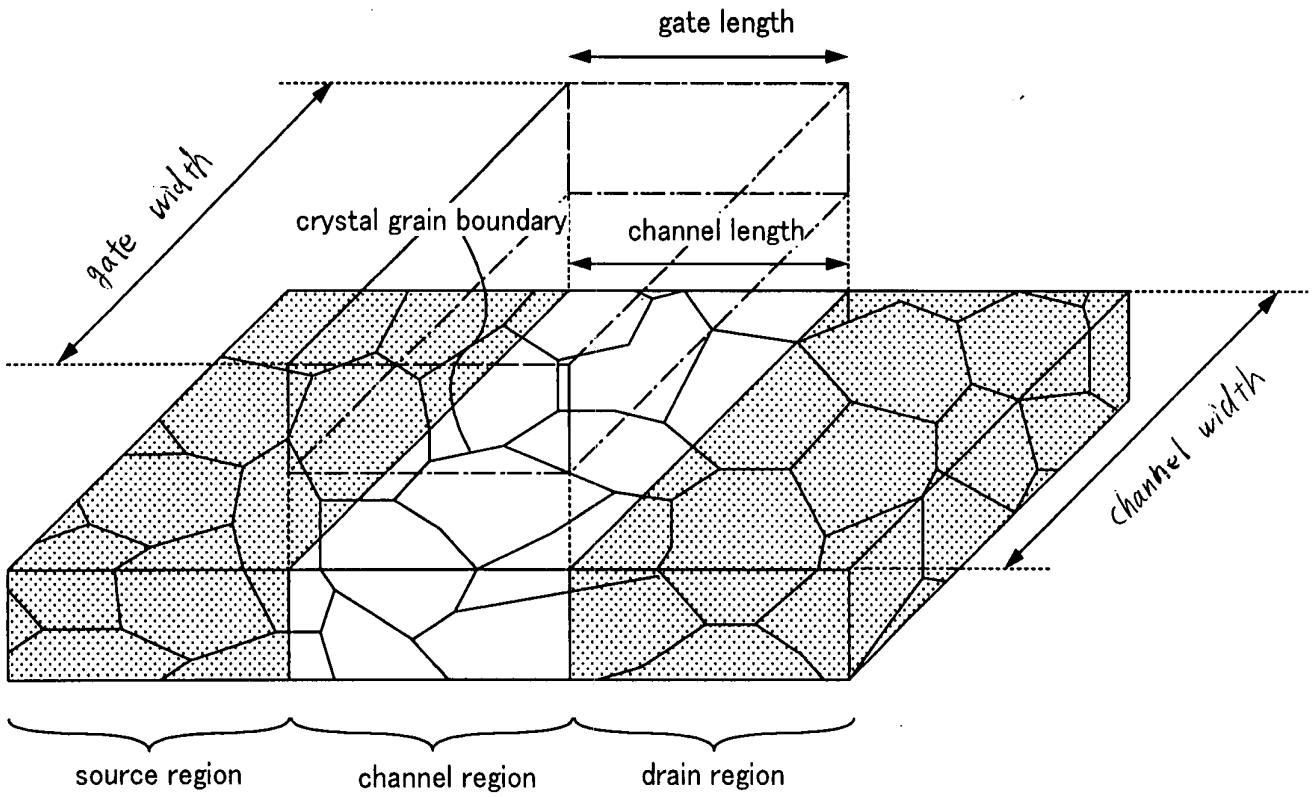


Fig. 15

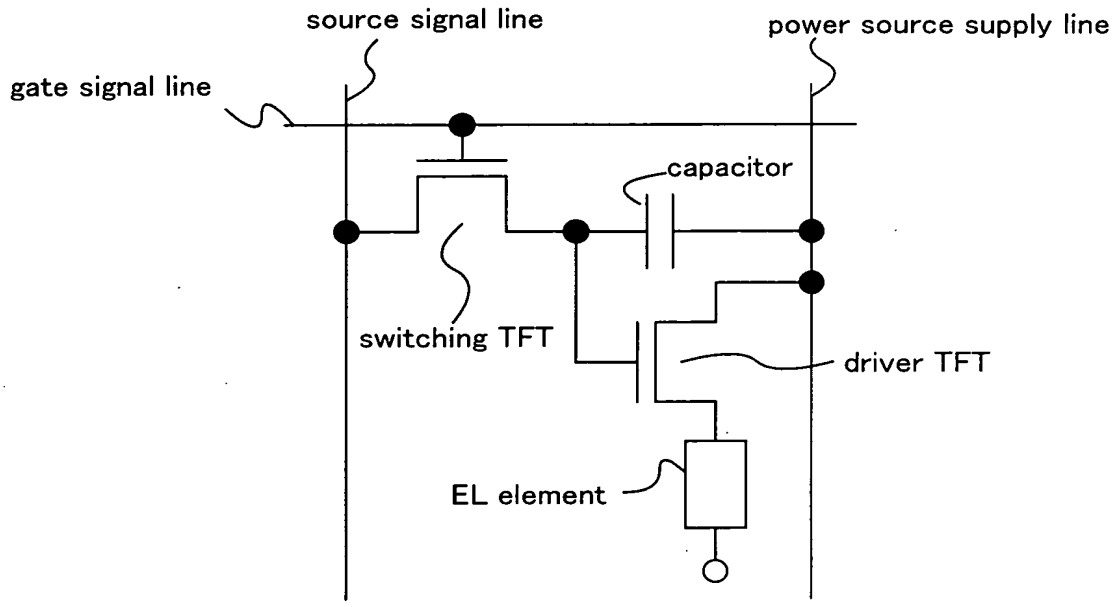


Fig. 16A

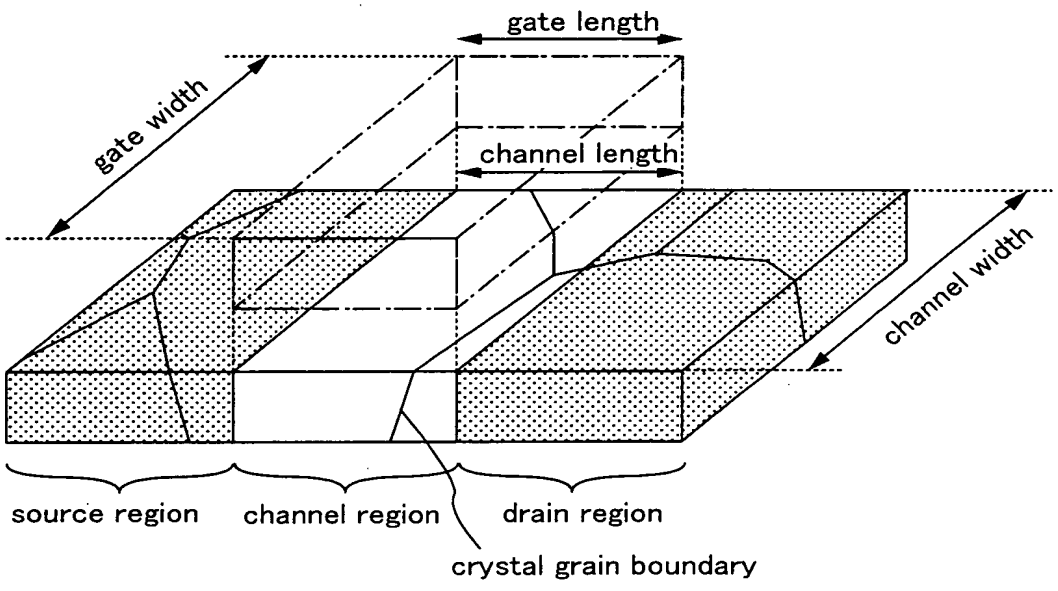


Fig. 16B

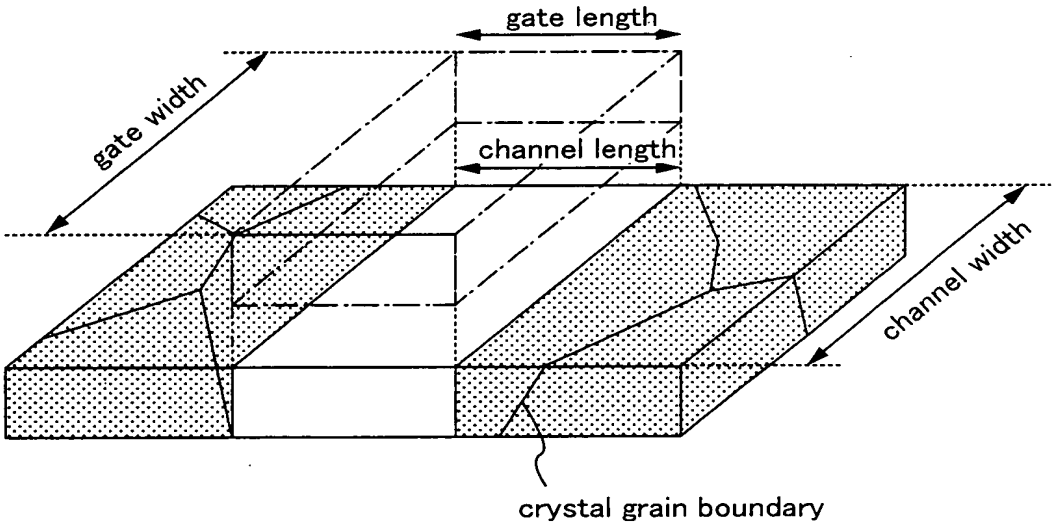


Fig. 17

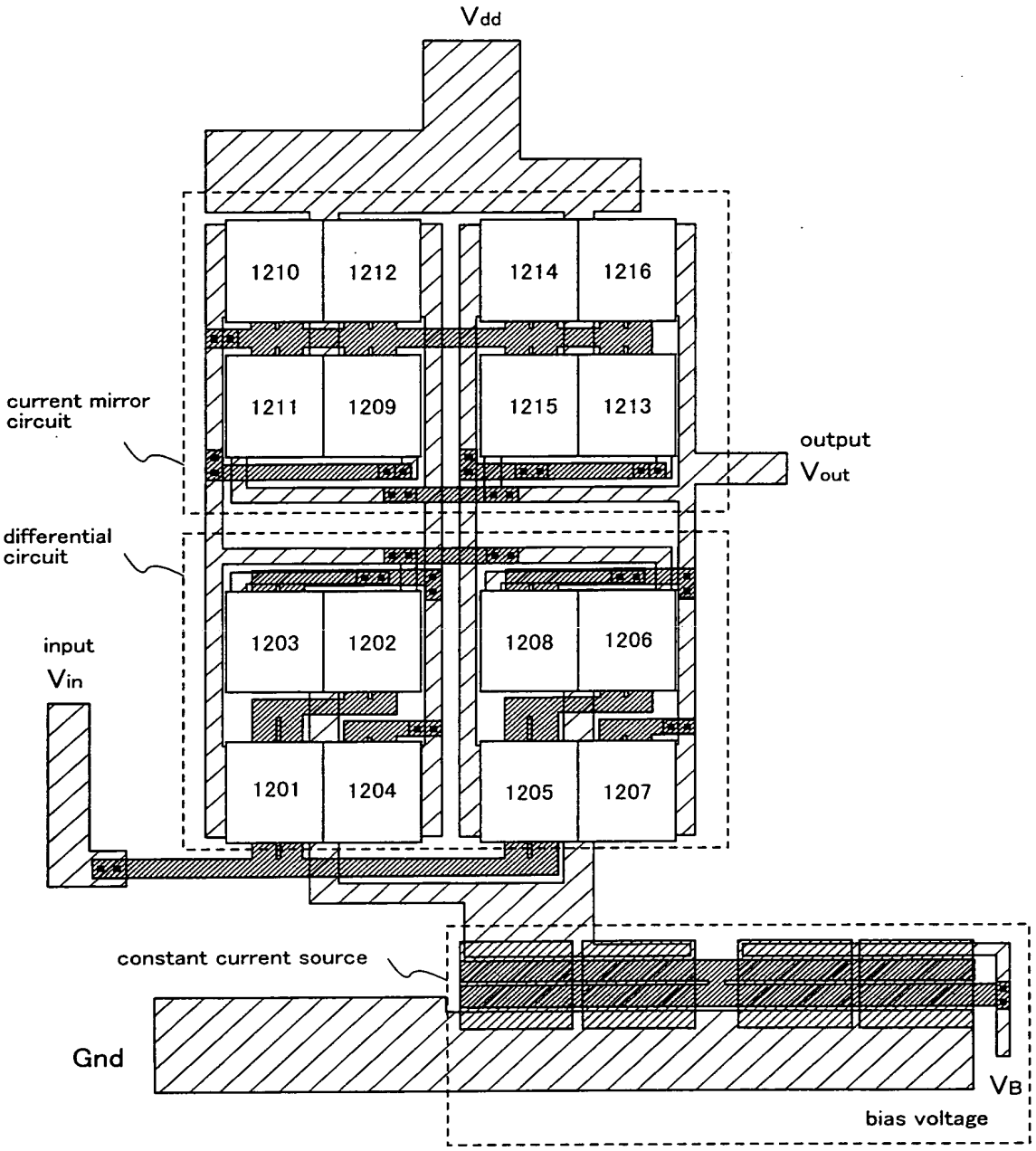

Vdd
1210
1212
1214
1216
1211
1209
1215
1213
current mirror circuit
output
Vout
differential circuit
1203
1202
1208
1206
input
Vin
1201
1204
1205
1207
constant current source
Gnd
VB
bias voltage

Fig. 18

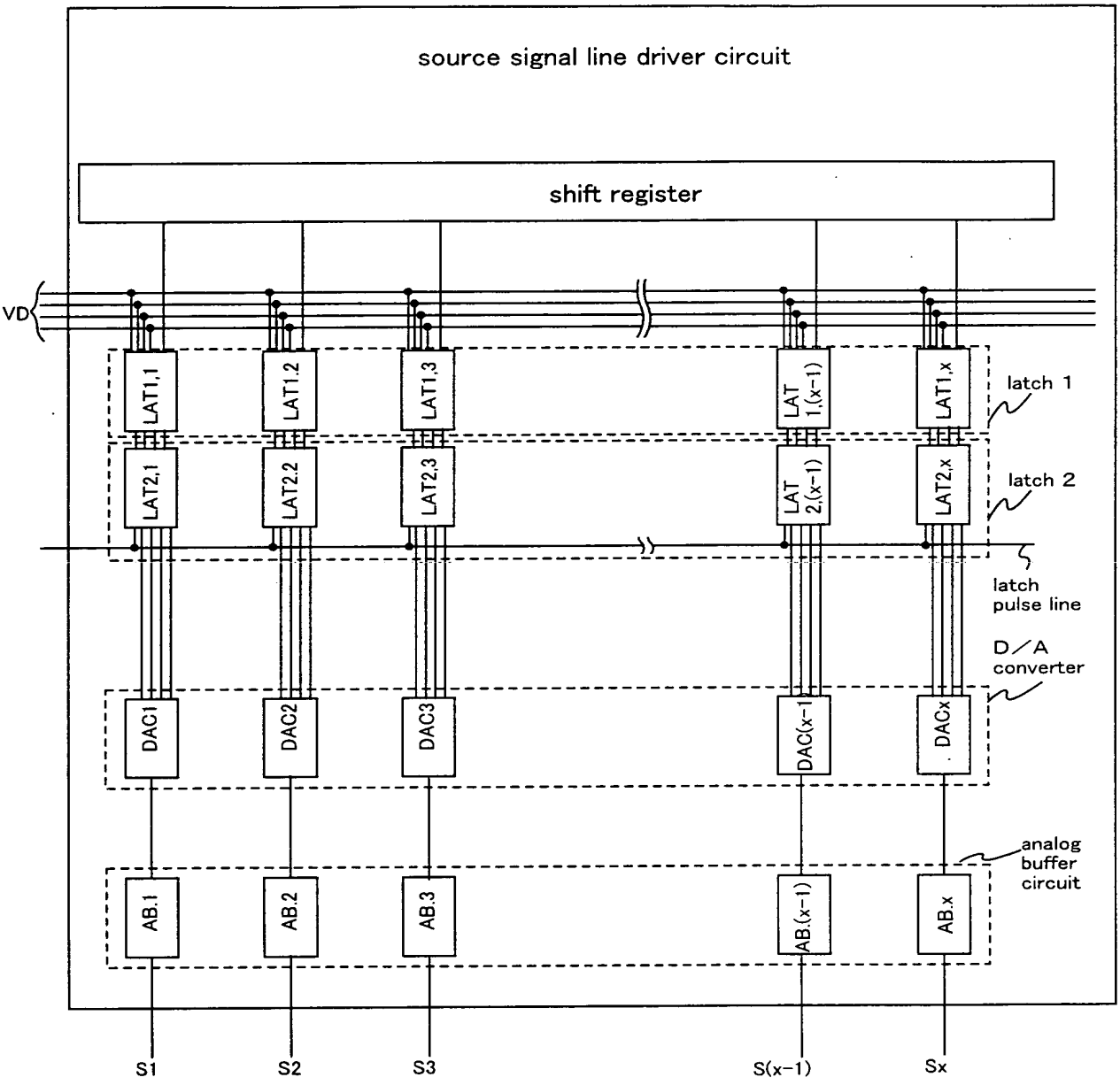
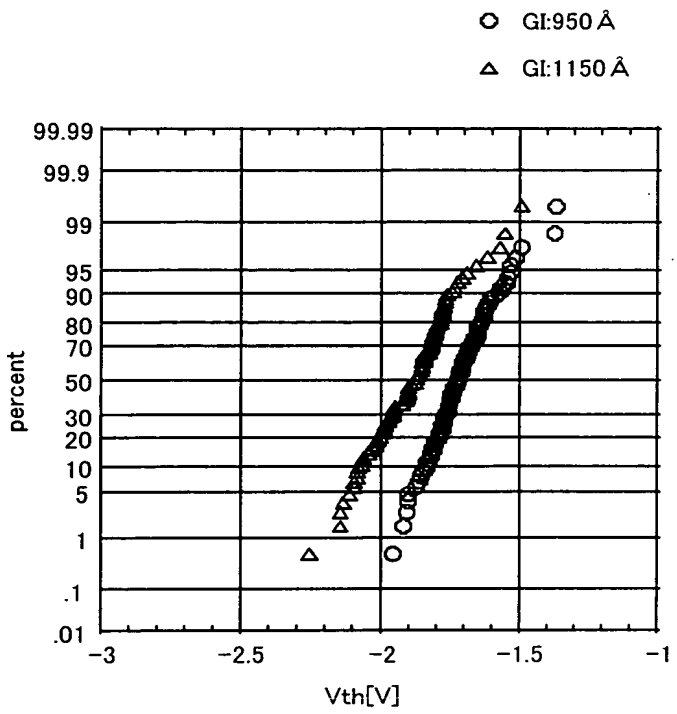
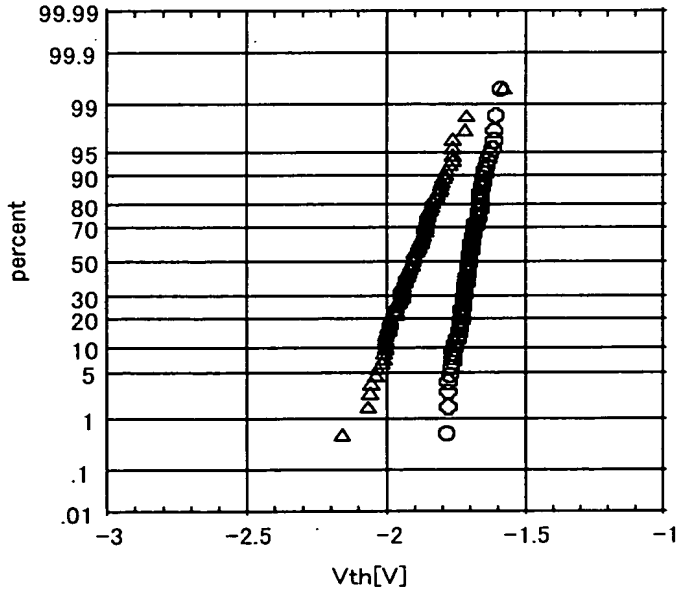

source signal line driver circuit
shift register
VD
LAT1,1
LAT1,2
LAT1,3
LAT 1,(x-1)
LAT1,x
latch 1
LAT2,1
LAT2,2
LAT2,3
LAT 2,(x-1)
LAT2,x
latch 2
latch pulse line
D/A converter
DAC1
DAC2
DAC3
DAC(x-1)
DACx
analog buffer circuit
AB.1
AB.2
AB.3
AB.(x-1)
AB.x
S1
S2
S3
S(x-1)
Sx

Fig. 19A



gate width is 8 μ m

Fig. 19B



gate width is 200 μ m

Fig. 20A characteristic of input and output in buffer circuit

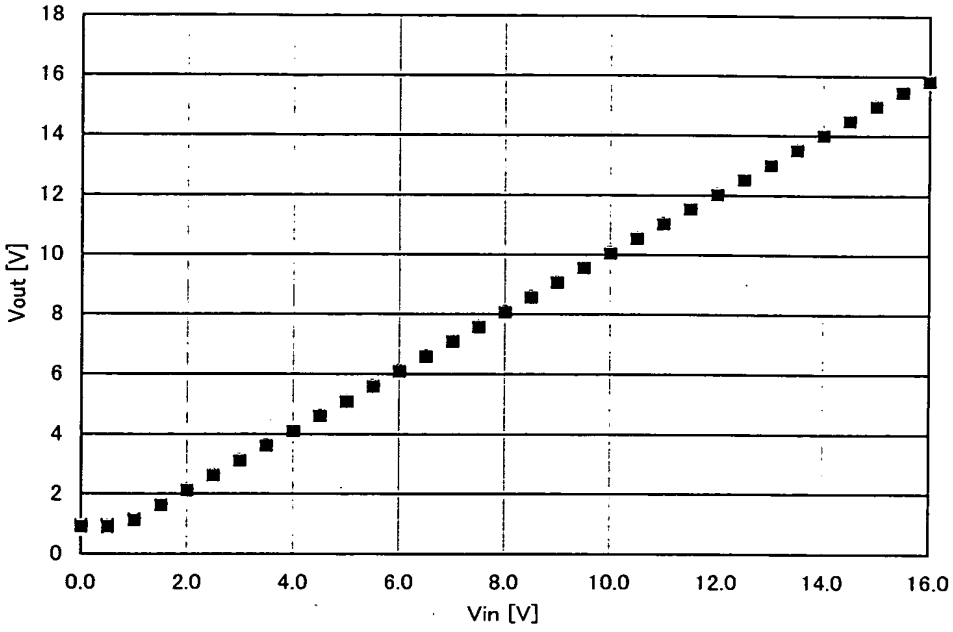


Fig. 20B

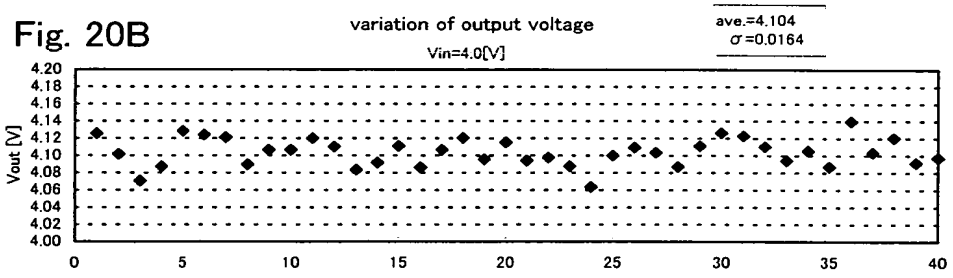


Fig. 20C

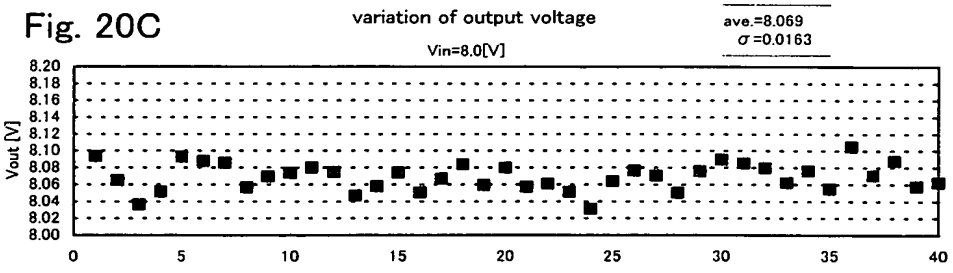


Fig. 20D

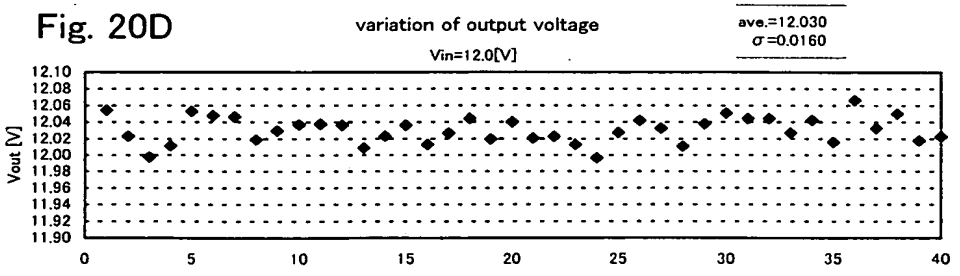


Fig. 21A semiconductor layer formation/insulating film formation/formation of first and second conductive films

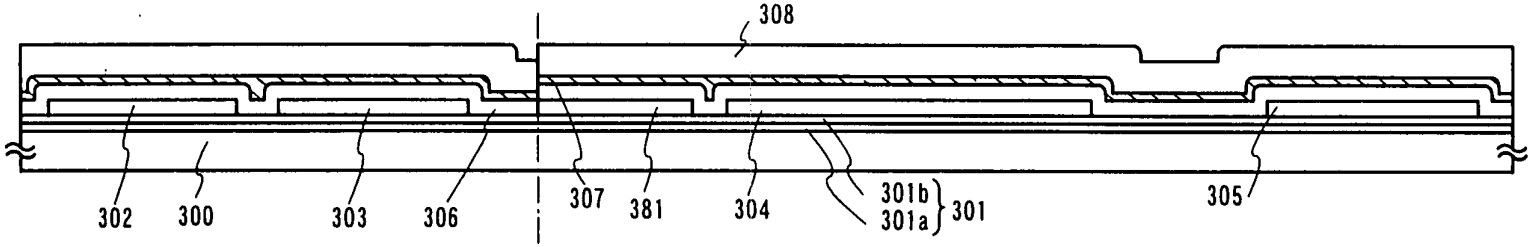


Fig. 21B first etching process/first doping process

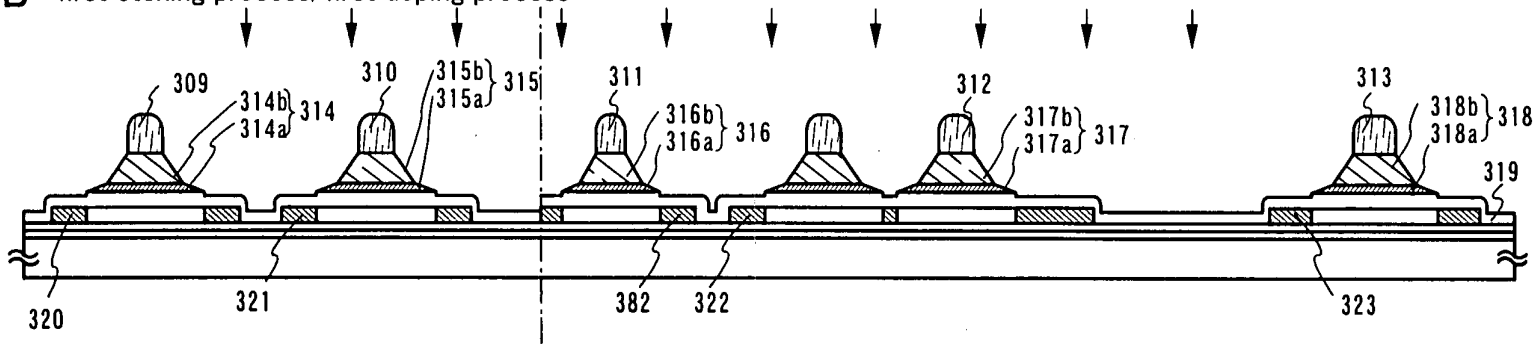


Fig. 21C second etching process

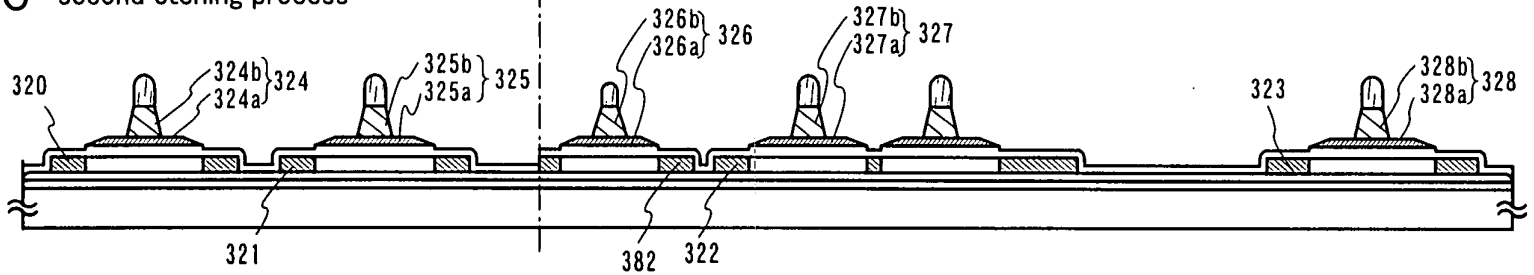


Fig. 22A second doping process

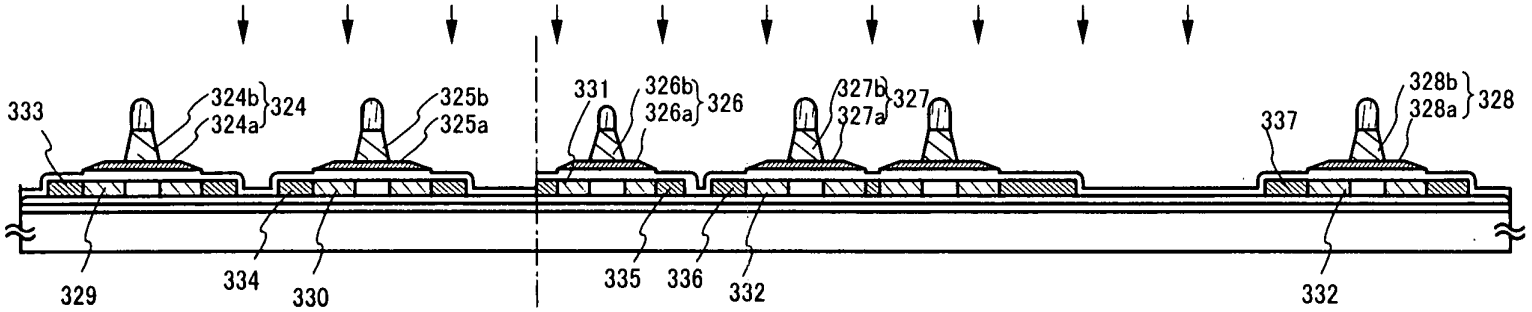


Fig. 22B third etching process

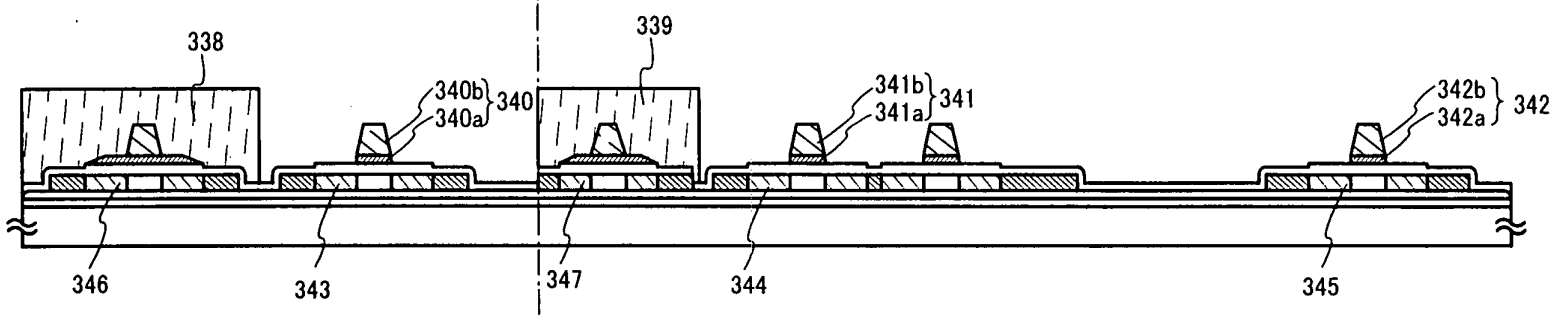


Fig. 22C third doping process

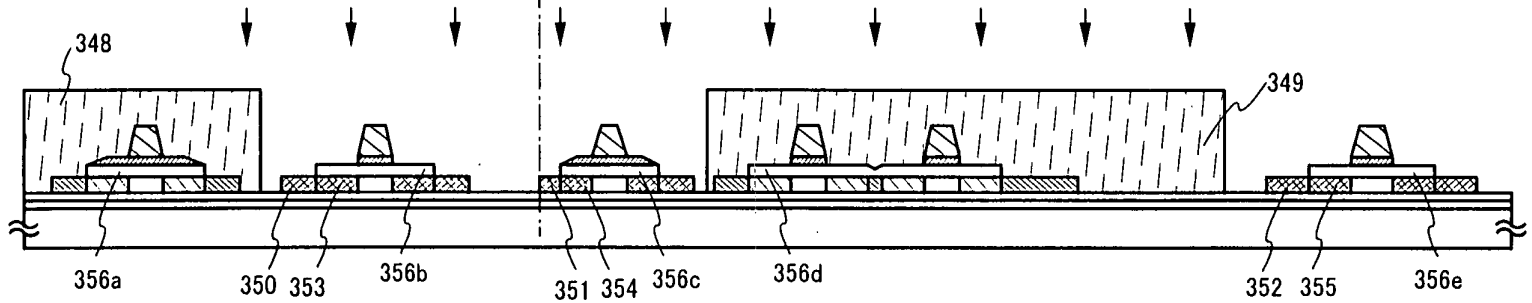


Fig. 23A formation of first interlayer insulating film, activating process

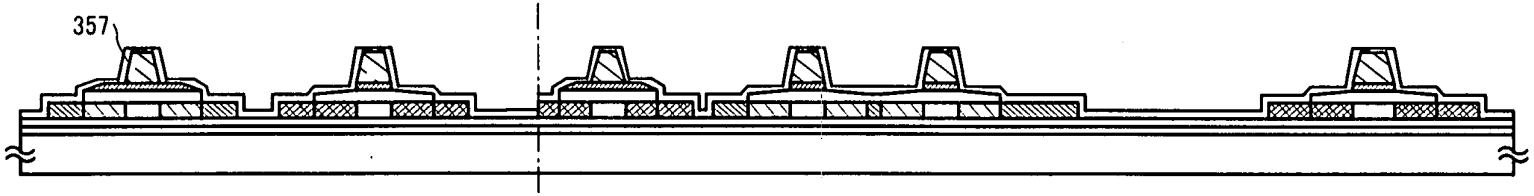


Fig. 23B formation of second interlayer insulating film, wiring, pixel electrode

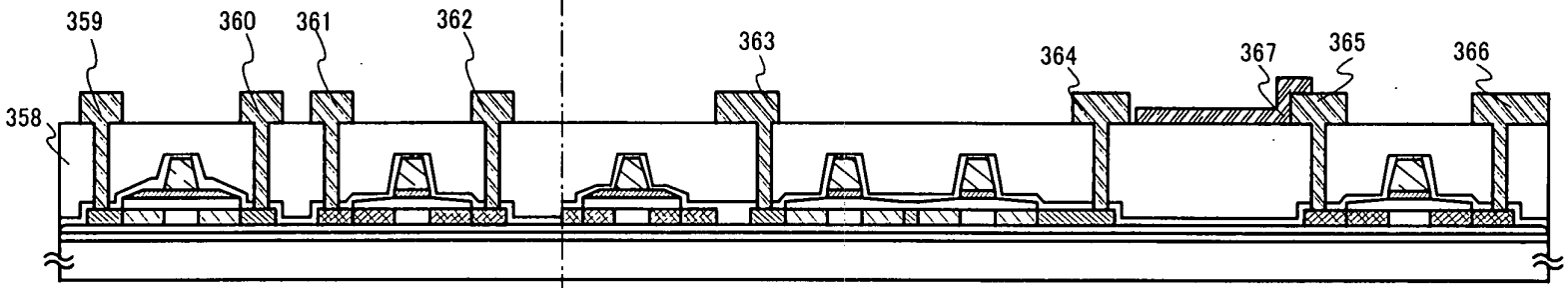
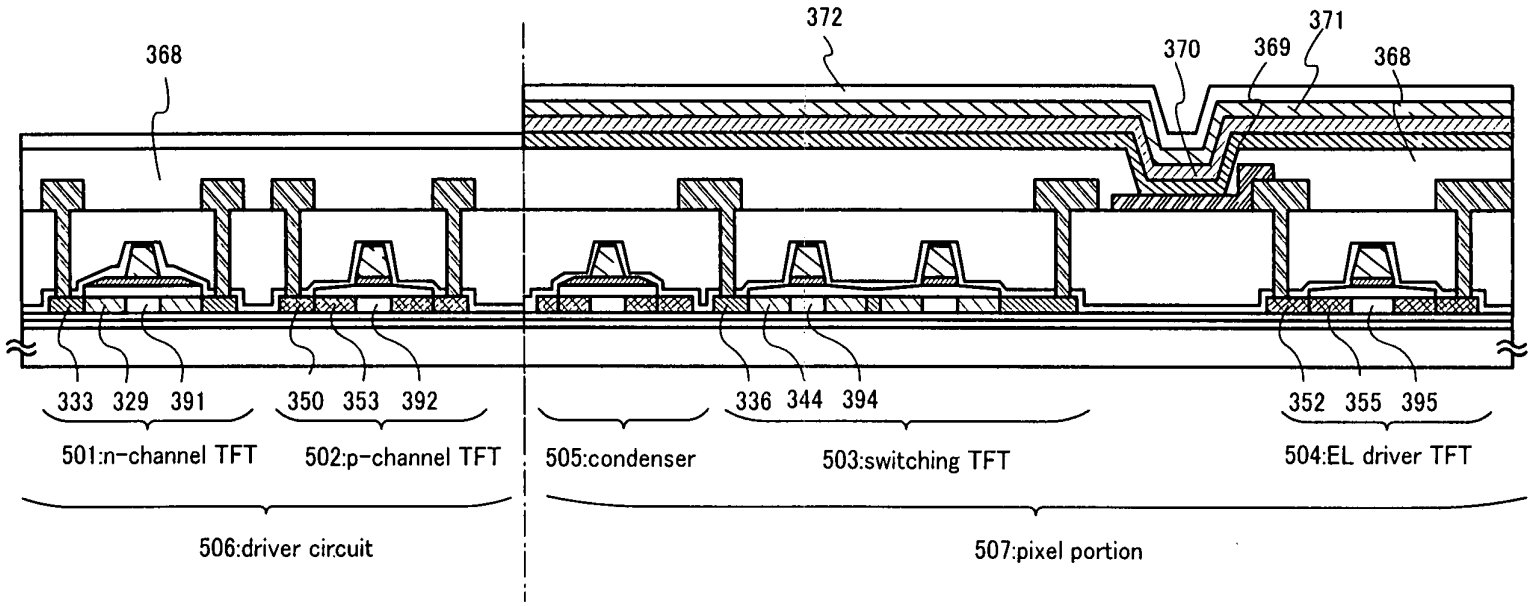


Fig. 24 formation of third interlayer insulating film, EL layer, pixel electrode, passivation film



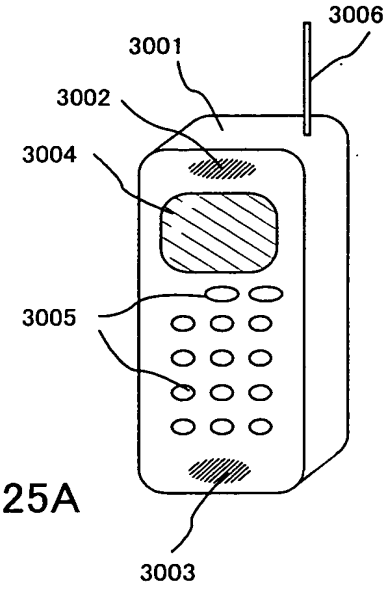


Fig. 25A

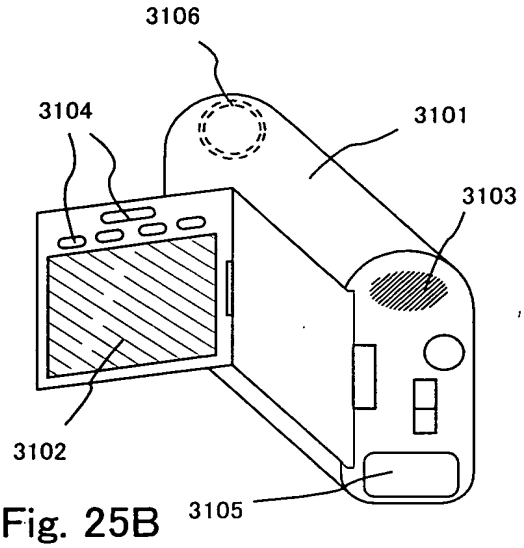


Fig. 25B

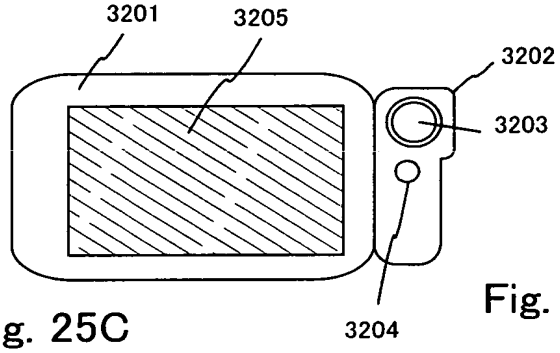


Fig. 25C

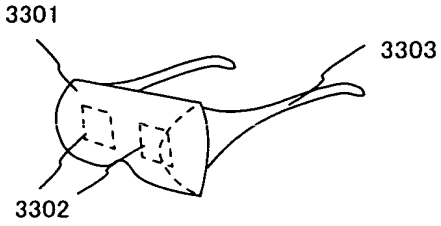


Fig. 25D

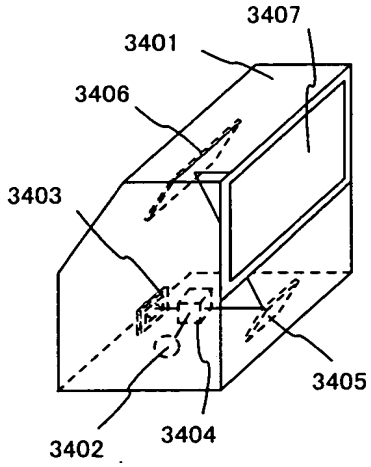


Fig. 25E

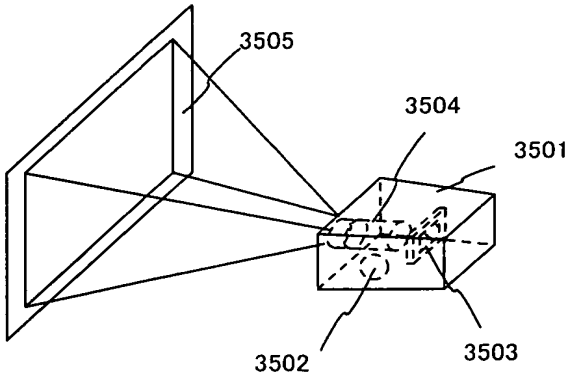


Fig. 25F